APPLICATION NOTE

- TDA8763AM/TDA8763M - 10-BIT A/D CONVERTER DEMONSTRATION BOARD

AN/98095

UPDATE

Philips Semiconductors

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- TDA8763AM/TDA8763M - 10-BIT A/D CONVERTER DEMONSTRATION BOARD

AN/98095

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SUMMARY

The **TDA8763** is a 10-bit high-speed low-power **A**nalog-to-**D**igital **C**onverter designed for professional video and other applications. It converts the analog input signal into 10 bits binary digital words or into two's complement digital words at a maximum sampling rate of 50Msps.

The reference voltage of the quantization ladder can be external with the **TDA8763AM** version or internal with the **TDA8763M** version.

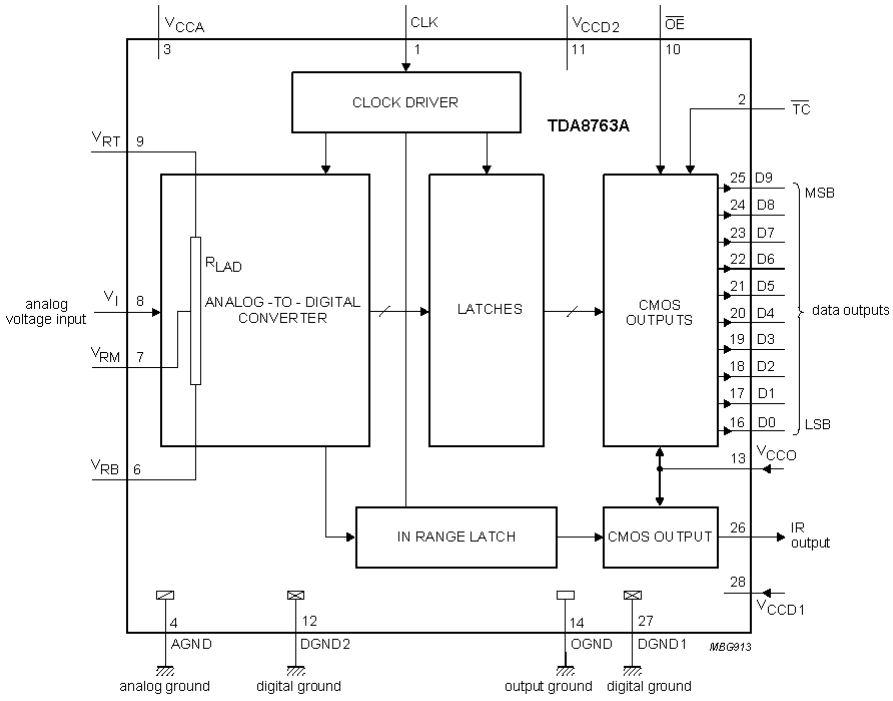
Three versions of this device exist: **TDA8763AM/3**, **TDA8763AM/4** and **TDA8763AM/5** (or **TDA8763M/3**, **TDA8763M/4** and **TDA8763M/5**) corresponding respectively to the clock frequency of 30Msps, 40Msps and 50Msps.

This **A**pplication **N**ote describes the design and the realization of the **Demonstration Board** (n° 618) using the **TDA8763AM** and **TDA8763M** versions with an application environment.

1. MAIN FEATURES OF THE TDA8763AM AND THE TDA8763M:

The **TDA8763AM** and the **TDA8763M** are 10-bit **A**nalog-to-**D**igital **C**onverters. They can convert a typical analog input signal into 10 bits binary coded digital words at a maximum sampling rate of 50 Mega sample per second with a typical power dissipation of 175mW for the **TDA8763AM** and 235mW for the **TDA8763M**. The **TDA8763AM** and the **TDA8763M** code either binary or two's complement digital words with 3V to 5V25 CMOS digital outputs. The **TDA8763M** contains an internal reference voltage regulator ensuring the TOP and the BOTTOM reference voltages of the quantization ladder. The block diagram and main specifications points of **TDA8763AM** device are shown on **Figure 1**.

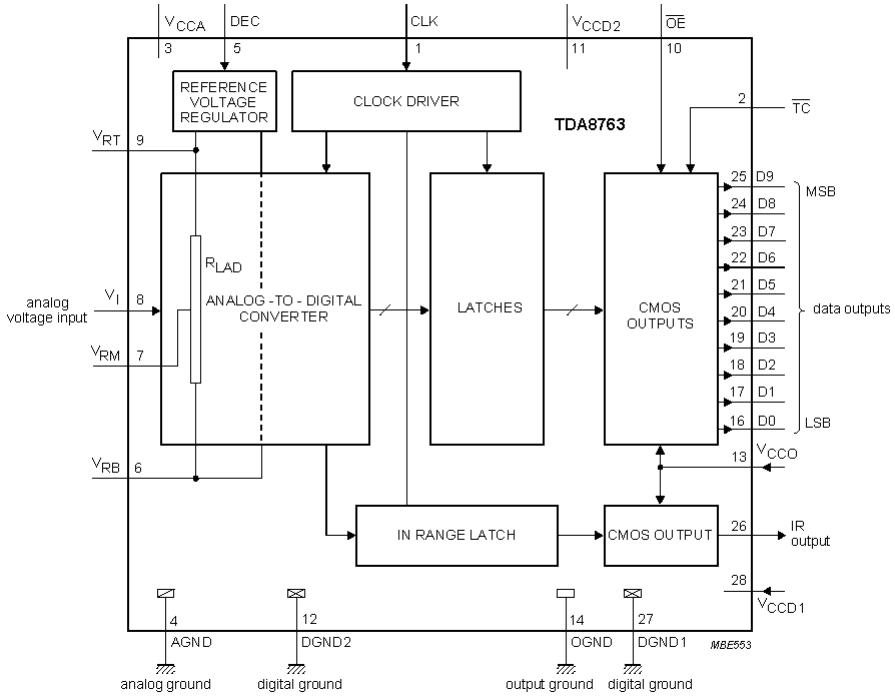
- Clock frequency: 30, 40 or 50Msps.
- Output voltage: 0V - 3V to 5V25.
  Power dissipation (typical): 175mW.
- Accuracy: 10-bit.
- Supply: 5V with output stages going from 3V to 5V25.
- Compatibility: input: TTL and CMOS
  output: TTL, CMOS (3V to 5V25).



- Figure 1. TDA8763AM block diagram -

The **TDA8763M** device includes an internal voltage reference regulator. The block diagram and main specifications points of this device are shown on **Figure 2**.

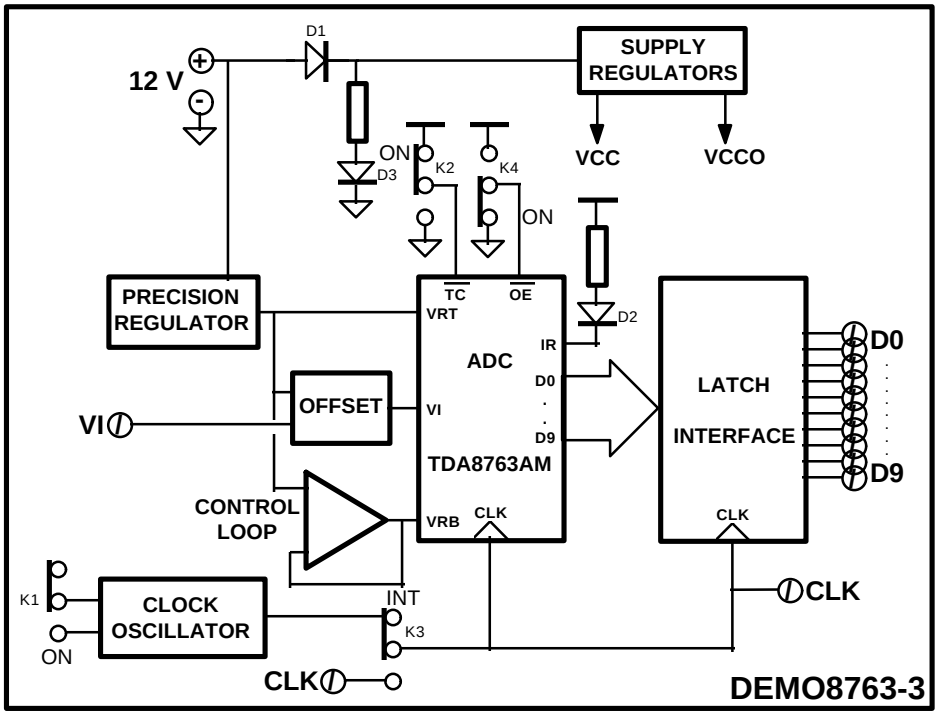
- Clock frequency: 30, 40 or 50Msps.
- Output voltage: 0V - 3V to 5V25.
  Power dissipation (typical): 235mW.
- Accuracy: 10-bit.
- Supply: 5V with output stages going from 3V to 5V25.
- Compatibility: input: TTL and CMOS
  output: TTL, CMOS (3V to 5V25).



- Figure 2. TDA8763M block diagram -

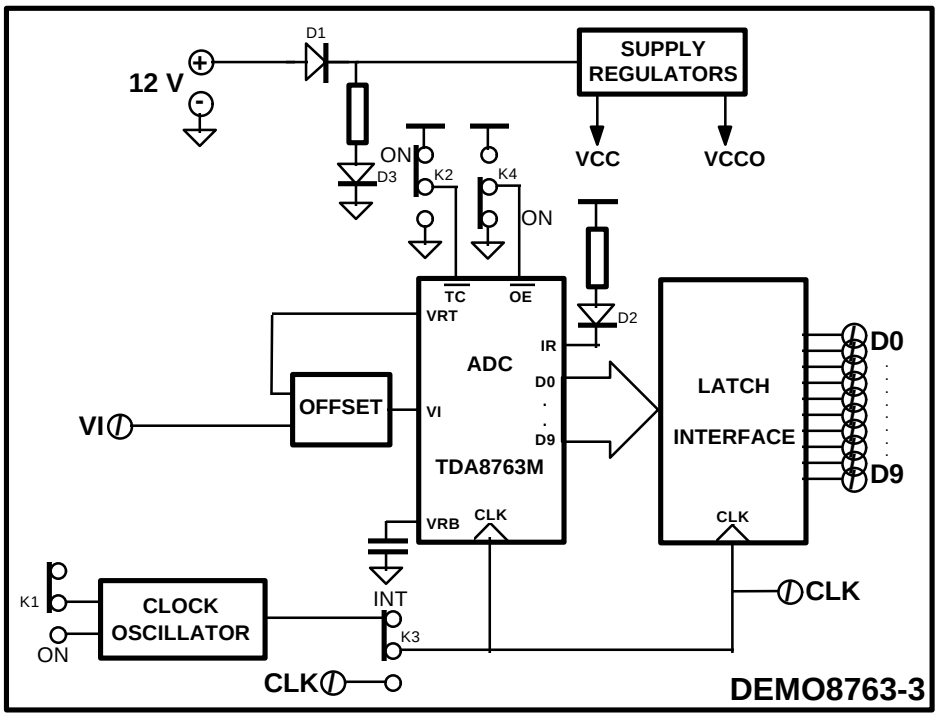
2. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board**, which is described in this **A**pplication **N**ote, is shown on **Figure 3** for the **TDA8763AM**.



- Figure 3. Functional block diagram of TDA8763AM Demoboard -

The same **Demoboard** is used for the **TDA8763M** and for the **TDA8763AM** but without an external precision regulator and a control loop. The block diagram of the **TDA8763M** application is shown on **Figure 4**.



- Figure 4. Functional block diagram of TDA8763M Demoboard -

The different blocks of the **Demoboard** are:

- A block of power **supply regulators** used to supply all the circuitry on the board.
- A voltage **precision regulator** (used for the **TDA8763AM** only) supplying the ADC reference voltage TOP input $\mathbf{V_{RT}}$ and polarising the control loop and the input bridge offset.
- A voltage **control loop** circuit (used for the **TDA8763AM** only) supplying the ADC reference voltage BOTTOM input $\mathbf{V_{RB}}$ of the quantization ladder, allowing to compensate the different thermal variations of the voltage values.
- A control **offset** bridge polarizing the ADC analog voltage input **VI**.

- A **latch interface** synchronising the ADC data output.

- A **clock oscillator** producing the internal clock on the **Demoboard** for the ADC and the latch interface.

The **Demoboard** works with a single $+12V_{DC}$ external power supply. All circuitry is protected from reverse polarity. The good supply plugging is indicated by a green LED.

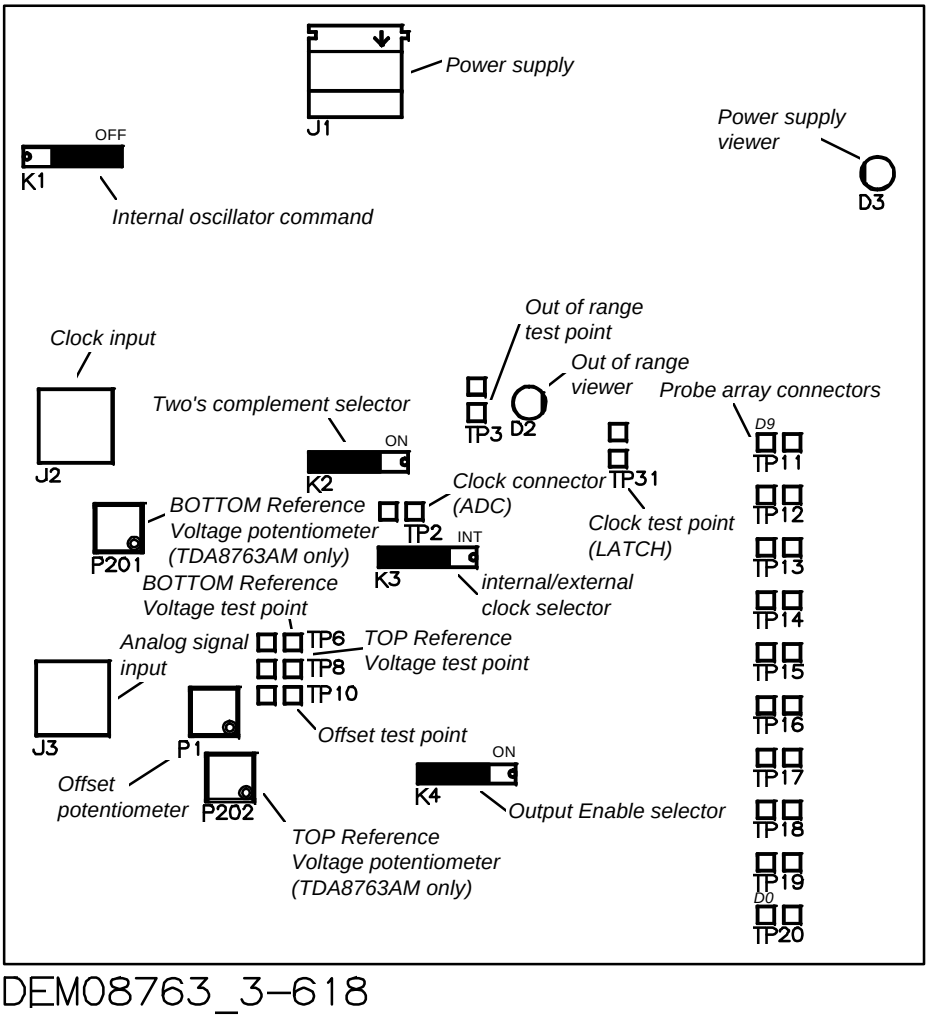
The overflow and the underflow of the input analog signal VI is indicated by a red LED.

The sample clock signal on the **Demoboard** can be internal, or it can be external by plugging the square generator in the **CLK** SMA connector. In this case the output impedance of this generator must be 50Ω.

To avoid the crosstalk when an external CLK is used, don't forget to switch off the clock oscillator.

3. OVERVIEW OF THE BOARD:

The whole implantation of this **Demoboard** is shown on **Figure 5**.



DEM08763_3–618

- Figure 5. Overview of Demoboard -

The different connectors, potentiometers, switches, lights and test-points available on the board are:

- **For the general power supply:**

1. A two-points PHOENIX connector **J1** for **$12V_{DC}$** and **GND**.
2. A green light **D3** to indicate the good supply plugging.

- **For the DC voltage adjustment values:**

1. Three chip potentiometers **P202**, **P201** and **P1** to adjust respectively the $\mathbf{V_{RT}}$ TOP reference voltage, the $\mathbf{V_{RB}}$ BOTTOM reference voltage and the $\mathbf{V_{OFS}}$ analog input offset of the ADC. **P202** and **P201** are available for the **TDA8763AM** only.
2. Three test-points **TP8**, **TP6** and **TP10** to control respectively the $\mathbf{V_{RT}}$ and $\mathbf{V_{RB}}$ reference voltages and $\mathbf{V_{OFS}}$ values.

- **For the evaluation of the TDA8763AM and the TDA8763M:**

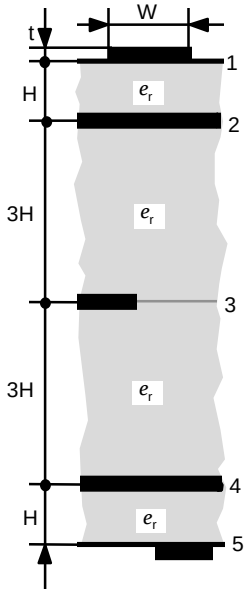
1. A SMA **J3** connector with 50Ω for the analog input signal **VI**.
2. A SMA **J2** connector with 50Ω for the external clock input **CLK**.
3. A switch **K1** to command the clock oscillator on/off.
4. A switch **K3** to choose the clock oscillator/external clock.
5. A switch **K4** to enable the ADC outputs by the input $\overline{\mathbf{OE}}$.
6. A switch **K2** to choose the ADC two's complement input $\overline{\mathbf{TC}}$.
7. A red light **D2** associated with the **TP3** indicating the out of range of the input analog signal.

- **For the reconstruction of the analog input waveform:**

1. Ten-probe array connectors **TP11** to **TP20** corresponding to the ADC digital output **D9** to **D0** are available to connect the logic analyser which computes the data.
2. A connector **TP2** corresponding to the ADC clock.
3. A test-point **TP31** corresponding to the latch interface clock.

4. PCB DESIGN:

The design was made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 6**.



- Figure 6. PCB structure -

Five physical copper layers are used. The first and fifth layers are the signal layers which contain the microstrip lines. The second and fourth layers constitute the ground planes corresponding to the signal layers. The third layer is designed specially for the power supply wires.

The metallic hole technique is employed to make all the necessary interconnections between the layers. The dielectric substrate used is an Epoxy Glass resin with a relative permittivity ($\boldsymbol{e_r}$) of 4.7 and a copper thickness (**t**) of 35µm (≈1.4mils). The substrate thickness (**H**) is ≈0.2mm (8mils) between the copper layers signal/ground.

4.1 MICROSTRIP LINES:

To calculate the width (**W**) of these 50Ω matched lines, the Kaup's relation is used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{e_r}+1.41}{87}}} - \frac{t}{0.8},$$

$$\text{(Accurate to within 5\% when } 0.1 < \frac{W}{H} < 3.0 \text{ and } 1 < e_r < 15\text{).}$$

where:

$Zo = 50\Omega$, $t = 35\mu m/\approx 1.4mils$, $H = 8mils/\approx 0.2mm$, $e_r = 4.7$.

4.2 POWER SUPPLY WIRE:

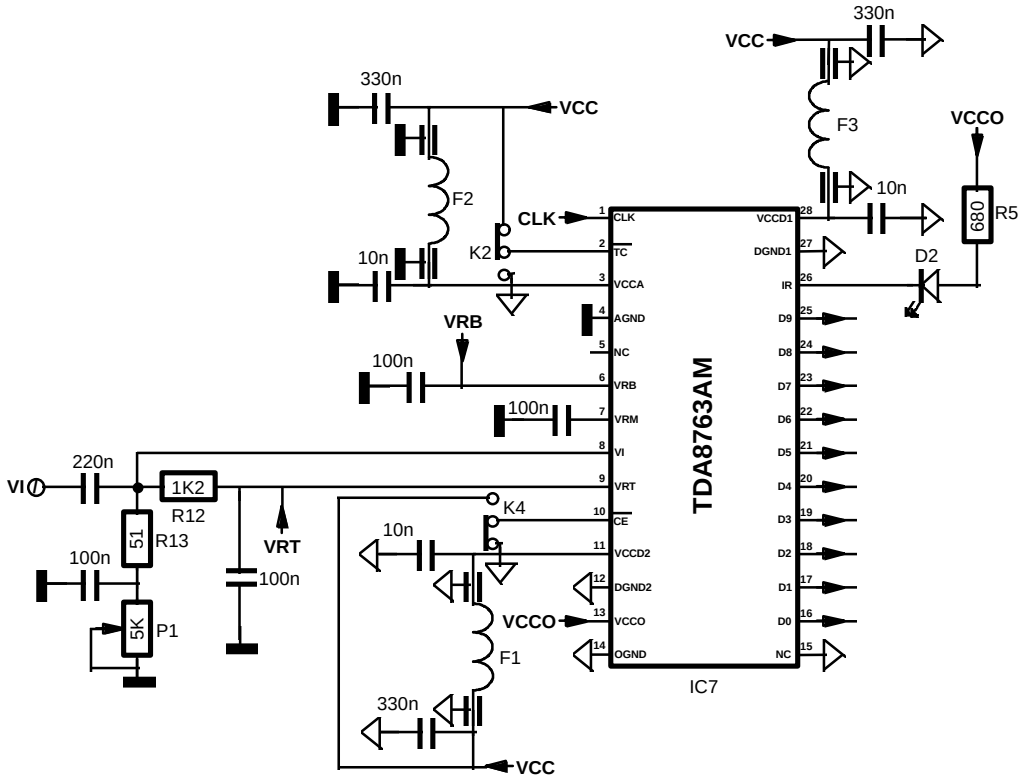
To reduce the voltage fluctuation effects due to switching currents inside the integrated circuits, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

4.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimise the noise due to capacitive coupling between the analog input and the digital output parts of the ADC, two separate ground planes are designed on all the layers of the **Demoboard** and they are connected together under the device.

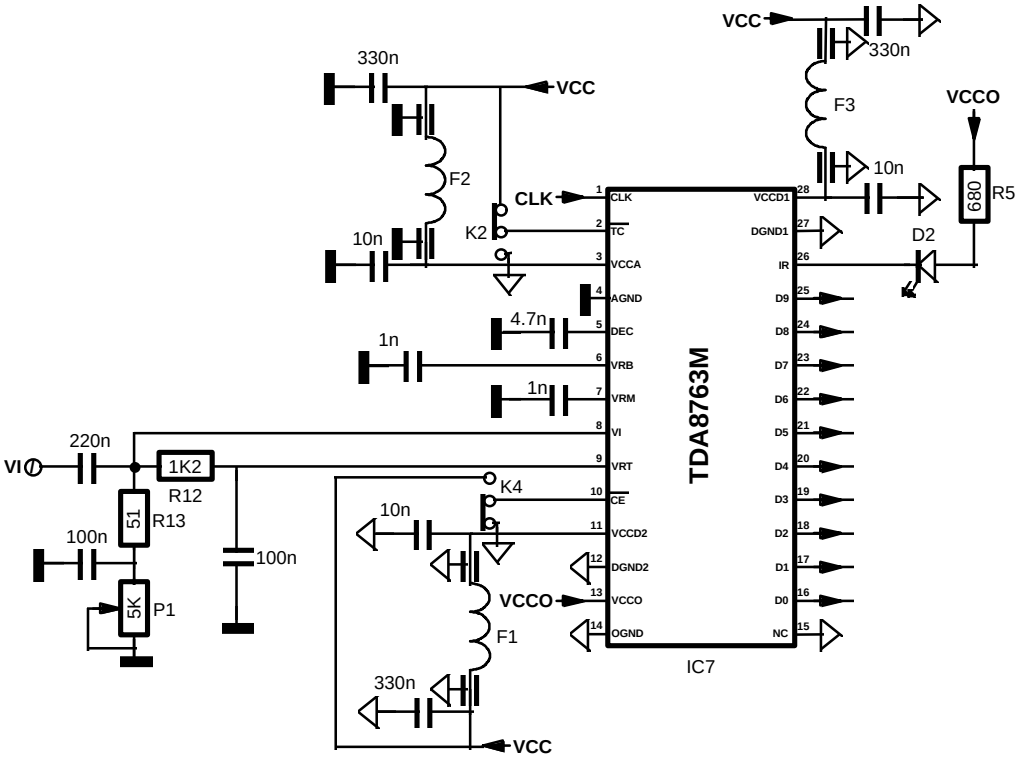
5. SPECIAL FEATURES OF THE APPLICATION BOARD:

To obtain optimal performances, the recommended application diagram is given on **Figure 7** for the **TDA8763AM**.



- Figure 7. TDA8763AM application diagram -

The recommended application diagram for the **TDA8763M** is given on **Figure 8**.



- Figure 8. TDA8763M application diagram -

5.1 ADC ANALOG INPUT VI:

The DC offset voltage is fixed on the board by an intermediate resistor bridge made by the resistors **R12** and **R13** associated with the potentiometer **P1**. The DC offset voltage value is adjusted from the $\mathbf{V_{RT}}$ reference voltage. This reference voltage is supplied either by the precision regulator for the **TDA8763AM** or by the internal reference voltage regulator for the **TDA8763M**.

So, the $\mathbf{V_{OFS}}$ typical offset voltage value (which corresponds to code 512) is obtained approximately from the relation:

$$V_{OFS} = \frac{V_{RT} + V_{RB} - V_{OST} + V_{OSB}}{2},$$

where:

V_{RT} = 3.67V (**TDA8763AM**),
V_{RT} = 3.6V (**TDA8763M**)
V_{RB} = 1.3V,
$V_{OST} = V_{OSB}$ = 0.175V.

Hence, the typical DC offset level $\mathbf{V_{OFS}}$ corresponding to code 512 is:

V_{OFS} = 2.485V (TDA8763AM),
V_{OFS} = 2.45V (TDA8763M).

To ensure a sufficient analog input stability, the offset resistor bridge current I_{VI} is fixed at 1mA. The value of **P1** is obtained by:

$$R13 + P1 = R12.\left(\frac{V_{OFS}}{V_{RT} - V_{OFS}}\right) \text{ and } R12 = \frac{V_{RT} - V_{OFS}}{I_{VI}},$$

where:

R13 = 50Ω.

The dynamic analog input is connected through a 220nF AC coupling to the external generator through a 50Ω microstrip line and a **R13** = 50Ω resistor ending.

A high frequency decoupling of 100nF is added to the potentiometer **P1** so that the decoupling allows to get a good dynamic ground.

The peak-to-peak magnitude nominal value $VI_{p.-p}$ of the dynamic input signal was determined from the relation:

$$VI_{p.-p} = V_{RT} - V_{RB} - V_{OST} - V_{OSB}.$$

Hence,

$VI_{p.-p}$ = 2.02V (TDA8763AM),
$VI_{p.-p}$ = 1.95V (TDA8763M).

The quantum is defined by:

$$q = \frac{VI_{p.-p}}{2^{10} - 1}.$$

Hence,

q ≈ 1.97mV (TDA8763AM),
q ≈ 1.91mV (TDA8763M).

5.2 DATA OUTPUT D0 TO D9:

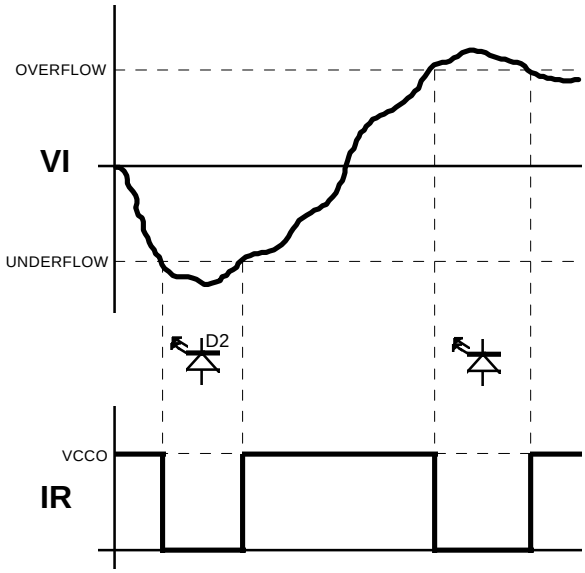
All data outputs of the **TDA8763AM** and of the **TDA8763M** are CMOS compatible and they are directly addressed to a latch interface circuit.

The switch **K2** corresponding to the two's complement input $\overline{\mathbf{TC}}$ allows the choice of either the binary digital words or the two's complement digital words.

The switch **K4** corresponding to the output enable input $\overline{\mathbf{OE}}$ allows either to enable or to put high impedance state on the data outputs.

5.3 DATA RANGE OUTPUT IR:

The underflow and overflow **IR** output pin is directly connected to the red light LED **D2**. When the underflow or overflow of the **VI** analog input signal is detected, the red LED is switched on. The functional diagram is shown on **Figure 9**.



- Figure 9. IR voltage waveform -

5.4 ADC ANALOG, DIGITAL AND OUTPUT STAGES POWER SUPPLIES:

Usually, a single power supply of 5V is necessary to supply the **TDA8763AM** and the **TDA8763M**. But on the **Demoboard**, the ADC is evaluated with a 3V3 voltage supply for the output stages.

To ensure a good bypassing at low and high frequency, the use of several different parallel capacitors is required and SMD bypass π type filters are implanted on the board near the ADC.

5.5 REFERENCE VOLTAGES VRB AND VRT (FOR THE TDA8763AM ONLY):

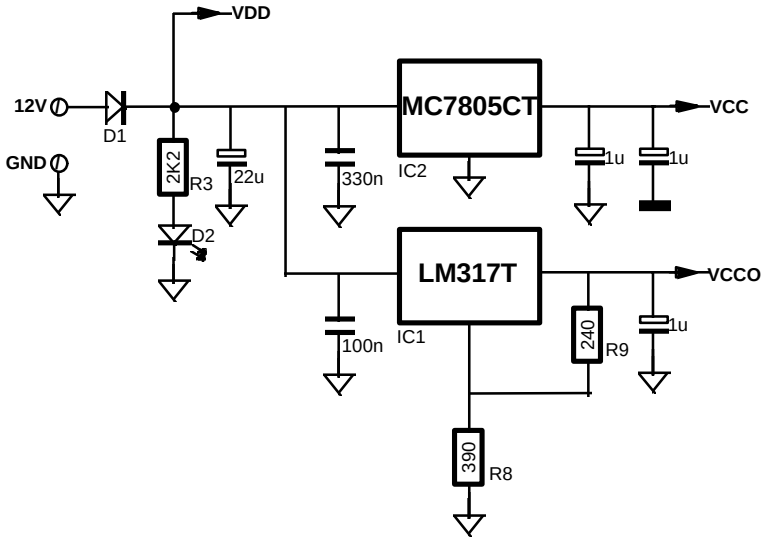
The TOP Reference Voltage $\mathbf{V_{RT}}$ of 3.67V is obtained from a specific IC precision voltage regulator implanted on the board. The regulator output voltage is directly applied on the $\mathbf{V_{RT}}$ pin of the ADC, a 100nF capacitor placed close to this point constitutes an effective decoupling.

The BOTTOM Reference Voltage $\mathbf{V_{RB}}$ of 1.3V is obtained by the **control loop** from a specific IC low voltage operational amplifier and a transistor. The output voltage of this **control loop** is directly applied on the $\mathbf{V_{RB}}$ pin of ADC.

6. ENVIRONMENT CIRCUITS:

6.1 GENERAL POWER SUPPLY:

The electric diagram is shown on **Figure 10**. Two IC voltage regulators **IC1** and **IC2** are used directly mounted on the board and they are supplied from an external DC power unit of $12V_{DC}$/210mA. Nevertheless, the external voltage can range from $10V_{DC}$ to $15V_{DC}$.



- Figure 10. Electric diagram of the power supply -

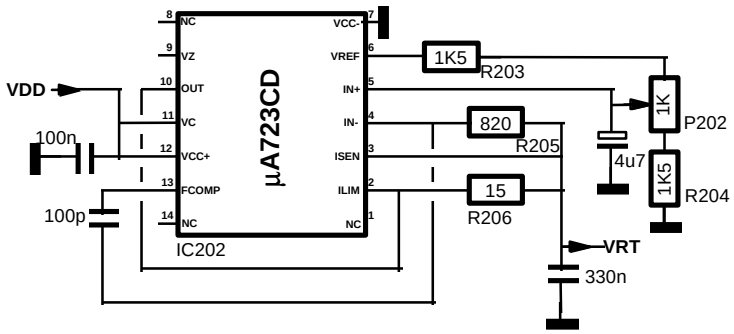
The regulation and the stabilisation of all circuitry come from the **VDD** voltage value obtained after the protection diode **D1**. Two stabilised voltages **VCC** of 5V and **VCCO** of 3V3 are available on the **Demoboard** with the distribution:

VCC used for:	**VCCO used for:**
Internal oscillator.	Latch interface.
ADC digital and analog supply voltages.	ADC output stages supply voltage.

The BYD17G Silicon diode **D1** ensures the protection of all the circuitry from reverse polarities, the good supply plugging is indicated by the green LED **D3**.

6.2 TOP REFERENCE VOLTAGE REGULATOR (AVAILABLE FOR THE TDA8763AM ONLY):

The precision voltage regulator **IC202 µA723CD** of PHILIPS SEMICONDUCTORS is used and mounted as a positive low-voltage regulator. The electric diagram used is shown on **Figure 11**.



- Figure 11. Electric diagram of the TOP reference voltage -

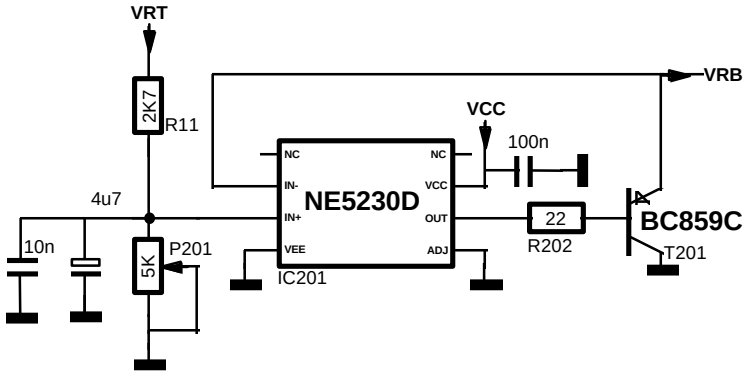
The voltage level **VDD** obtained on the cathode of the protection diode **D1** is applied on the VCC+ (pin 12) of this device.

The nominal reference level of 3.67V is obtained from the voltage level supplied on the VREF (pin 6) of the **µA723CD**. A bridge resistor **R203** and **R204** with a potentiometer **P202** allows to adjust the reference level value on the non-inverting input IN+ (pin 5) of the IC.

The frequency compensation of the output current amplifier stage is done with an external capacitor of 100pF connected between FCOMP (pin 13) and IN- (pin4).

6.3 BOTTOM REFERENCE VOLTAGE (AVAILABLE FOR THE TDA8763AM ONLY):

The low voltage operational amplifier **IC201 NE5230D** associated with the transistor PNP **T201 BC859C** of PHILIPS SEMICONDUCTORS are used and mounted as a control loop stage. The electric diagram used is shown on **Figure 12**.



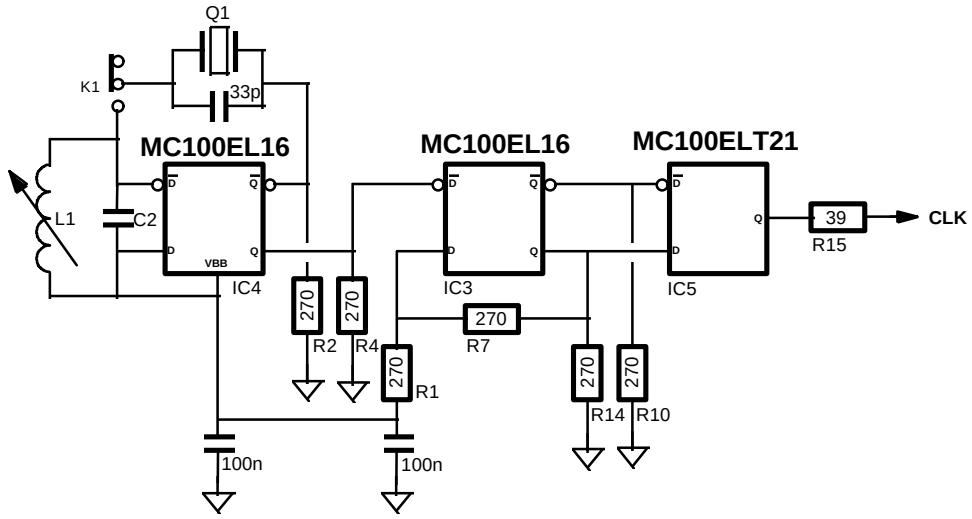
- Figure 12. Electric diagram of the BOTTOM reference voltage -

The $\mathbf{V_{RB}}$ voltage, controlled by the trimmer potentiometer **P201**, is applied on IN+ of **IC201** and is compared to IN- reference voltage of ADC to compensate the different thermal variations of the voltage values due to the quantization ladder.

The voltage output of the operational amplifier allows to control the conduction of the transistor **T201** which drives the current of the quantization ladder to GND. A resistor **R202** is therefore provided on the board to limit the output current in **IC201**.

6.4 CLOCK OSCILLATOR:

On the **Demoboard**, a specific circuit is designed to produce the clock signal addressed to ADC and to the latch interface circuit with the Motorola IC "ECL in PS" family. This is used to design a PECL mounting crystal oscillator. The electric diagram is shown on **Figure 13**.

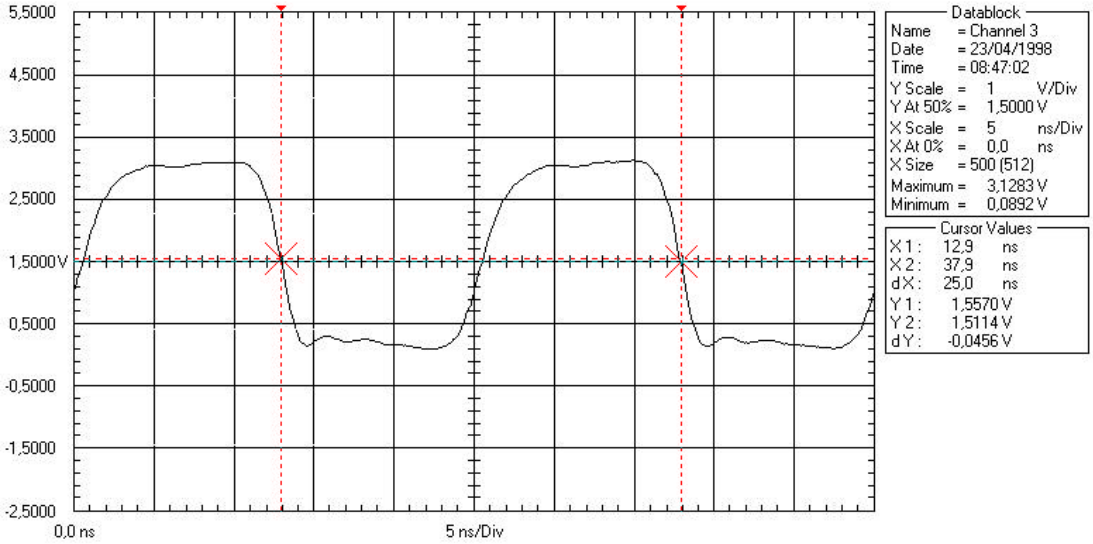


- Figure 13. Electric diagram of the clock oscillator -

Two differential receivers **MC100EL16** are used to make the function of oscillating and shaping. The first differential receiver is associated in positive feedback with the quartz **Q1**. The antiresonance harmonic frequency is selected from the tuned inductance **L1** of the tank circuit **L1-C2**.

The first differential receiver output drives the input of Schmitt trigger circuit constituted by the second differential receiver **IC3** and by the associated resistors **R1** and **R7**. The second differential receiver output drives the **IC5** differential PECL to the TTL translator **MC100ELT21**.

The waveform of the clock oscillator signal obtained at 40Msps is shown on **Figure 14**.



- FIGURE 14. Clock oscillator waveform -

Depending on the ADC type implanted on the Demoboard (**TDA8763AM** or **TDA8763M** version **/3**, **/4** and **/5**), the values of the quartz **Q1** and capacitor **C2** are:

ADC type and version:	**Q1:**	**C2:**
TDA8763AM/3-TDA8763M/3	32MHz	390pF
TDA8763AM/4-TDA8763M/4	40MHz	220pF
TDA8763AM/5-TDA8763M/5	50MHz	120pF

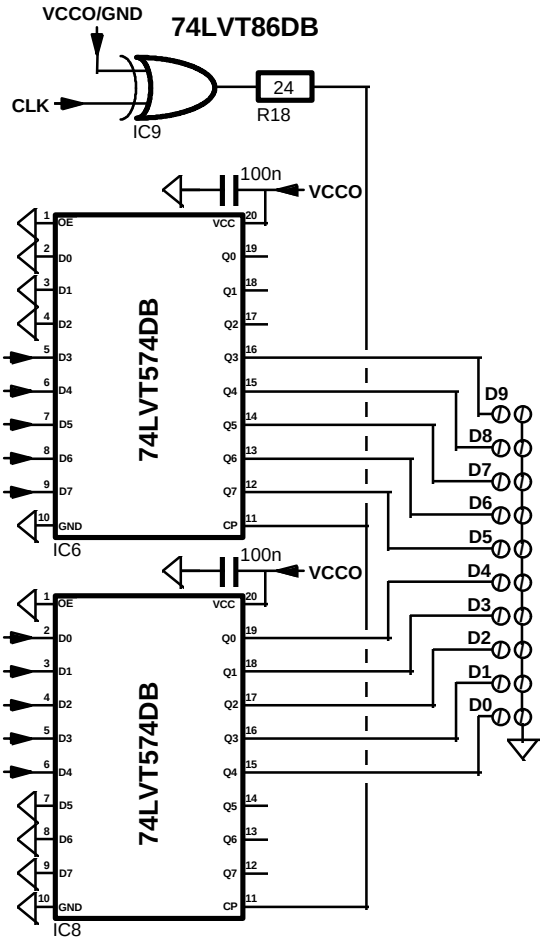
6.5 CLOCK SELECTOR CIRCUIT:

The position of the **K1** and **K3** switches 1C/2P on the **Demoboard** must be set on **ON** and **INT** to use the internal clock oscillator and **K1** and **K3** must be set on **OFF** and **EXT** to use the external generator which is connected to **J3** SMA connector.

To avoid the crosstalk when the external CLK is used, don't forget to switch off K1.

6.6 LATCH INTERFACE:

The electric diagram of the latch interface is shown on **Figure 15**. It allows to recover the ADC data output synchronised on the clock sampling.



- Figure 15. Electric diagram of the latch interface -

The interface circuit uses two SMD ICs D-type flip-flop **74LVT574DB** and an exclusive-or gate **74LVT86DB** from the Low Voltage Technology logic lamily.

7. OPERATING MODE:

An external power unit of 12V/210mA is required to supply the **Demoboard**. However, the board is able to work between 10V and 15V.

All DC voltage adjustments of **P202** (V_{RT}), **P201** (V_{RB}) and **P1** (V_{OFS}) are locked in the laboratory before delivery to be true to the provided product specifications. The **P202** and **P201** are available for the **TDA8763AM** only)

So, for the **TDA8763AM**:

V_{RT} = **3.67 V**,

V_{RB} = **1.30 V**,

V_{OFS} = **2.485 V**.

And for the **TDA8763M**:

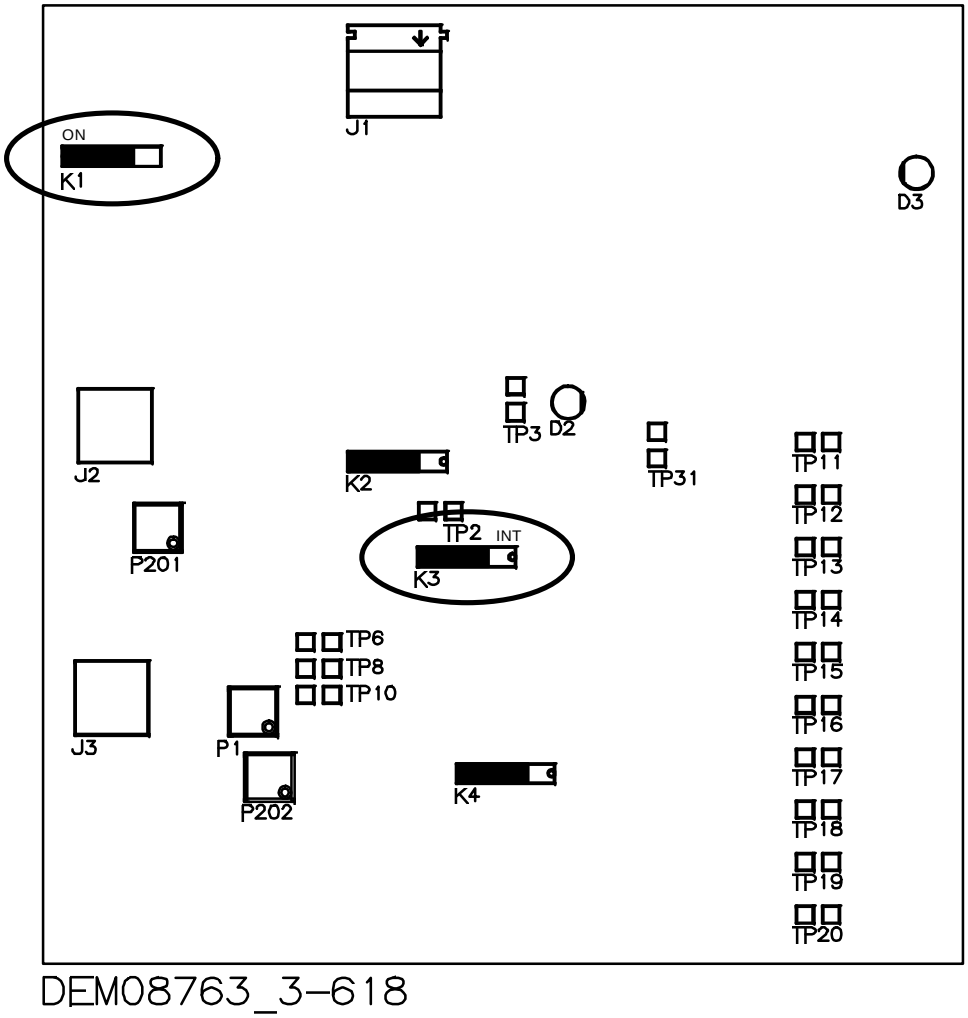
V_{OFS} = **2.45 V**.

But the V_{OFS} value may be modified by the user to obtain the best full scale of the input analog signal. To do this, it is better to use the IR viewer to check if the analog input signal is out of range. In this case, the LED **D2** switches on.

Before putting the board on, please check that **K1** is **OFF**, **K2** and **K4** are **ON**, and **K3** is **INT** (referring to the implantation diagram given on **Figure 5**).

7.1 INTERNAL CLOCK OPERATION:

In this mode, the different positions of the switches are given on **Figure 16**. To switch **ON** the internal clock oscillator, use switch **K1** once the board is powered on.

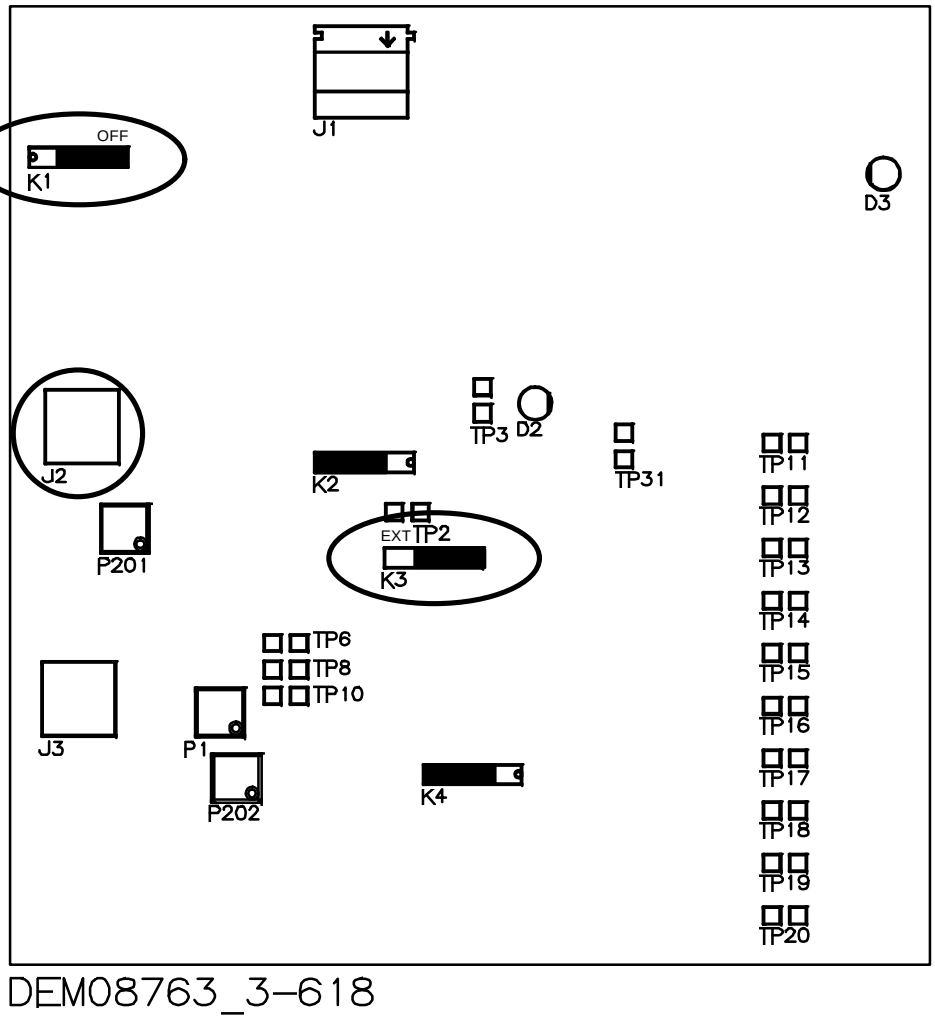


- Figure 16. Board configuration using the clock oscillator -

7.2 EXTERNAL SINGLE CLOCK OPERATION:

In this mode, the position of the different switches and the location of the connector and the location of connector are given on **Figure 17**.

- The internal clock oscillator command is set on **OFF** with the switch **K1** to avoid crosstalk.
- The external clock oscillator is set on **EXT** with the switch **K3**.
- The 50Ω SMA connector **J2** is used to connect the external 50Ω square clock generator.



- Figure 17. Board configuration using an external clock -

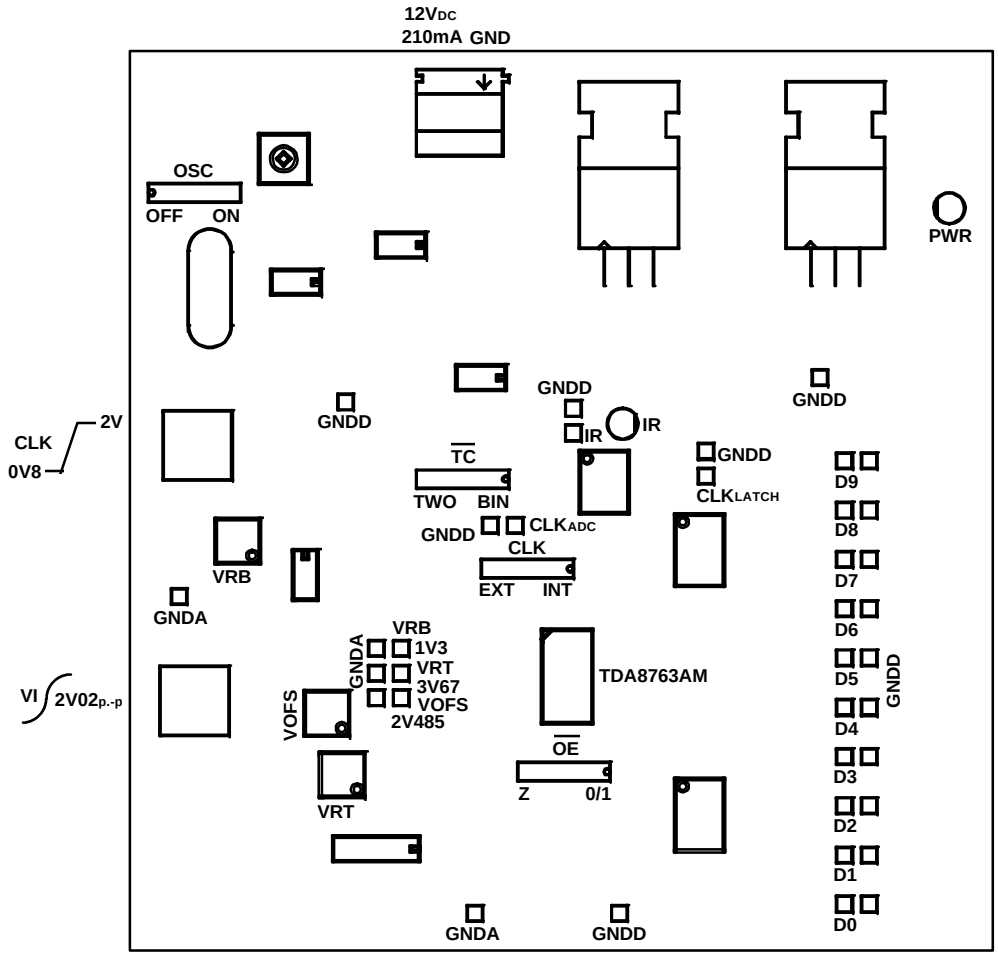
The required clock levels are:

V_{CLKH} min = 2.0 V,

V_{CLKL} max = 0.8 V.

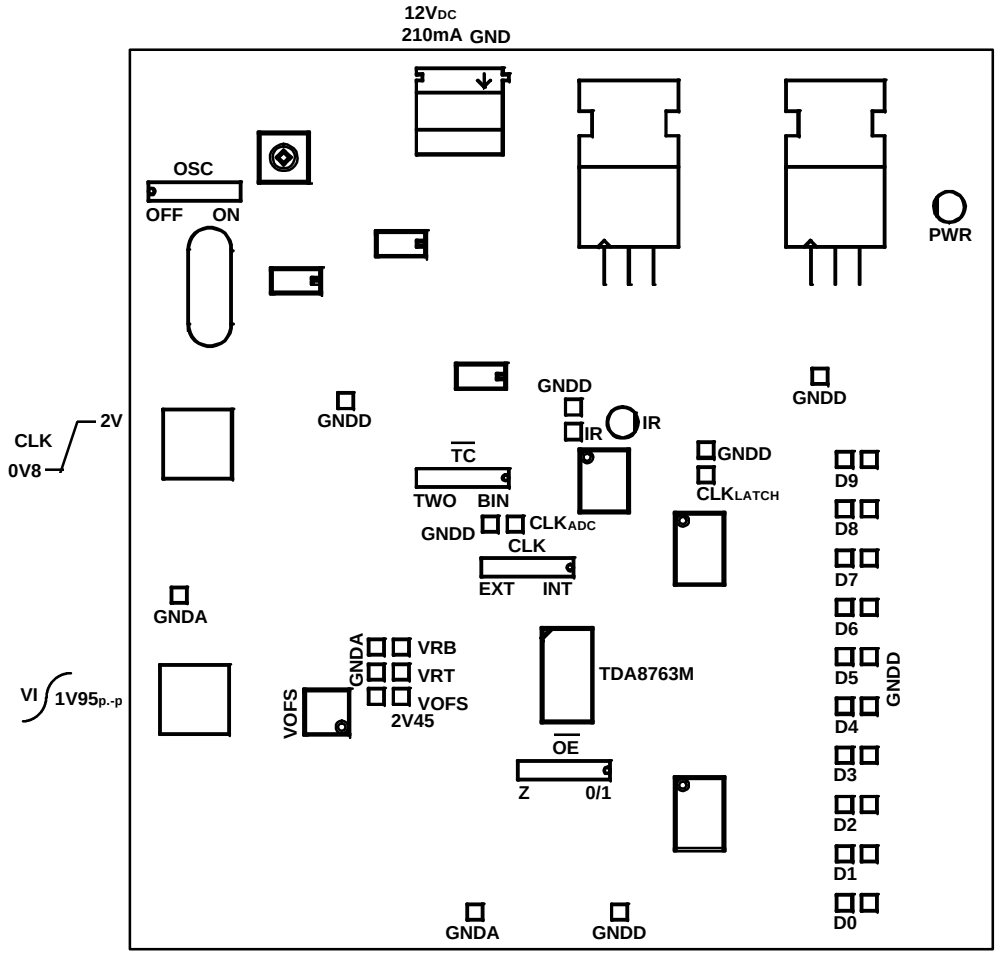
7.3 QUICKVIEW OF THE DEMOBOARD:

A quick view of the **TDA8763AM Demoboard** with main information is given on **Figure 18**.



- Figure 18. Quickview of the TDA8763AM Demoboard version with main information -

A quick view of the **TDA8763M Demoboard** with main information is given on **Figure 19**.



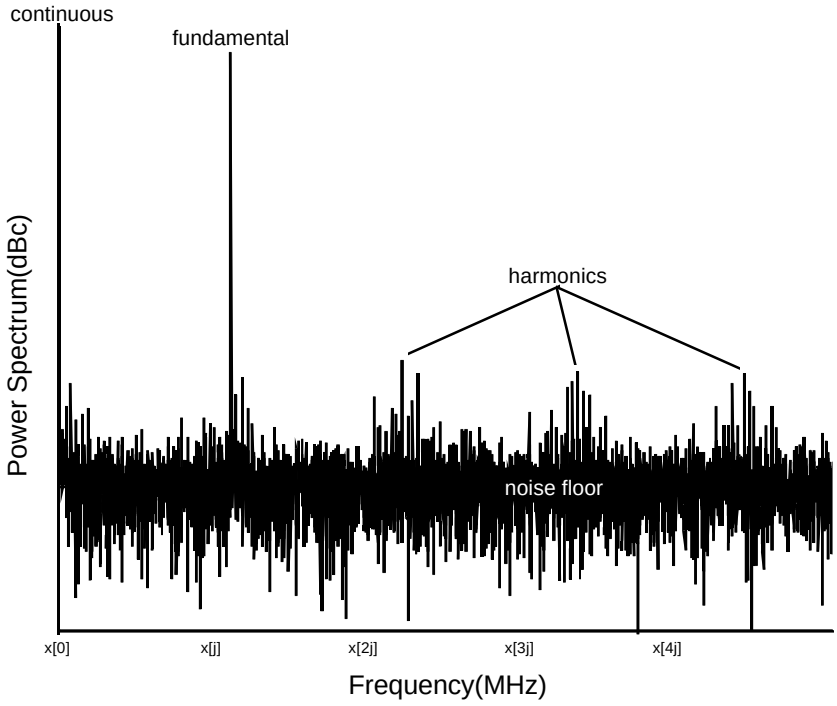
- Figure 19. Quickview of the TDA8763M Demoboard version with main information -

8. PERFORMANCES:

An evaluation of the performances of the **TDA8763AM** and the **TDA8763M** ADC was made with the **Demoboard** environment. Three versions were evaluated on the CAEN dynamic bench.

8.1 DEFINITION OF THE MEASURING PARAMETERS:

To evaluate the performances of ADC on the Demoboard, the CAEN dynamic bench uses the **F**ast **F**ourier **T**ransform for dynamic parameters from the sample signal.



- Figure 20. FFT -

According to the FFT shown on **Figure 20**, the main dynamic parameters are:

- The **T**otal **H**armonic **D**istortion is the ratio between the RMS signal amplitude and the RMS sum of the first five harmonics. From the power spectrum of FFT, the **THD** is calculated from the relation:

$$THD_{dBc} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2}^{6} x^2[i \times j]}}.$$

Where:

x[j] : fundamental component corresponding with the j spectrum component,

x[i × j] : component of harmonic i.

- The **S**purious **F**ree **D**ynamic **R**ange is the ratio between the RMS signal amplitude and the RMS value of the highest spectrum component (harmonic or noise). From the FFT, the **SFDR** is calculated from the relation:

$$SFDR_{dB} = 20 \times \log_{10} \frac{x[j]}{MAX(x[i])}.$$

Where:

x[i] : spectrum component i with $i \in [2:\frac{N}{2}]$ (N: number of samples) and $i \neq x[j]$.

- The **SI**gnal to **N**oise **A**nd **D**istortion ratio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components. From the FFT, the **SINAD** is calculated from the relation:

$$SINAD_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j}^{\frac{N}{2}} x[i]}}.$$

- The **S**ignal to **N**oise **R**atio is the ratio between the RMS signal amplitude and the RMS sum of all the other spectral components without harmonic used in the **THD** relation. From the FFT, the **SNR** is calculated from the relation:

$$SNR_{dB} = 20 \times \log_{10} \frac{x[j]}{\sqrt{\sum_{i=2, i \neq j \times [1:6]}^{\frac{N}{2}} x[i]}}.$$

- The **E**ffective number of bit is calculated by the relation (valid to NYQUIST condition):

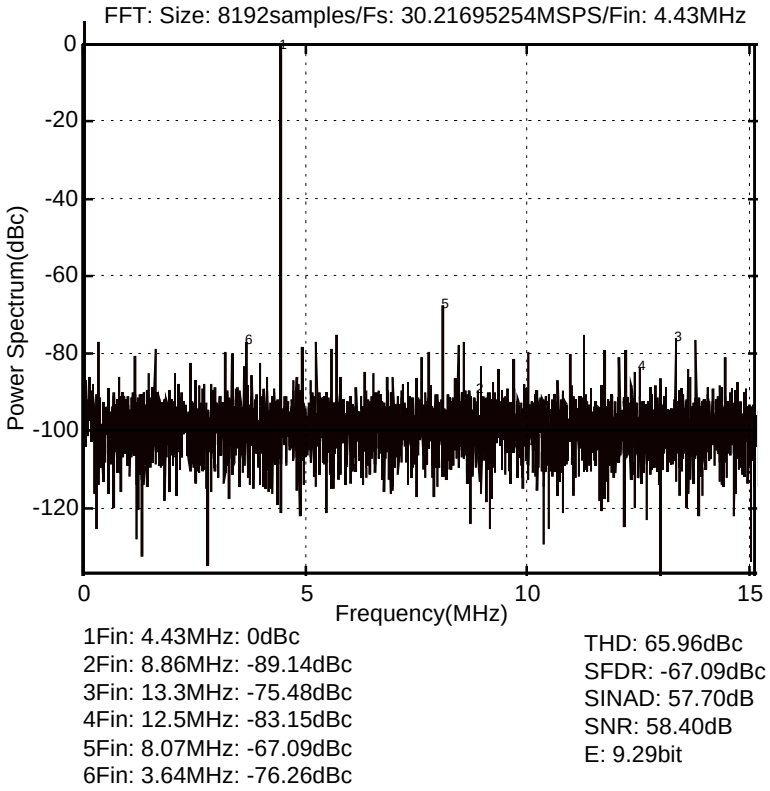
$$E_{BIT} = \frac{SINAD - 10 \times \log_{10} \frac{3}{2}}{20 \times \log_{10} 2}.$$

8.2 MEASUREMENT OF THE 30MSPS VERSION:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	4.43MHz.
Waveform:	Sinus.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes.
Clock frequency:	30.217Msps.
Operating mode:	External clock.

The typical results and the corresponding diagram obtained with these conditions are given on **Figure 21**:



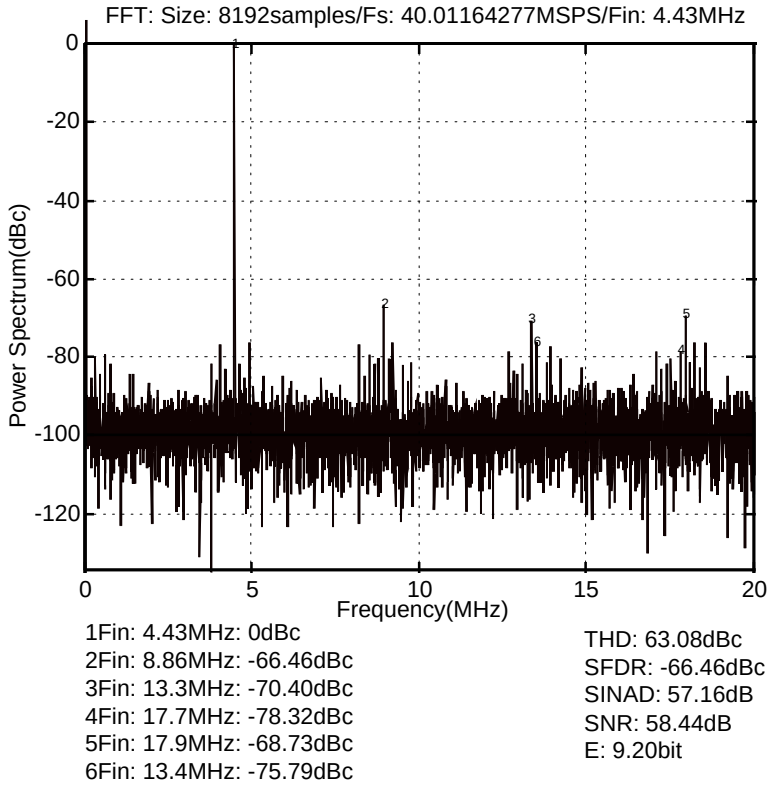
- Figure 21. Results of the 30Msps version -

8.3 MEASUREMENT OF THE 40MSPS VERSION:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	4.43MHz.
Waveform:	Sinus.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes.
Clock frequency:	40.012Msps.
Operating mode:	External clock.

The typical results and the corresponding diagram obtained with these conditions are given on **Figure 22**:



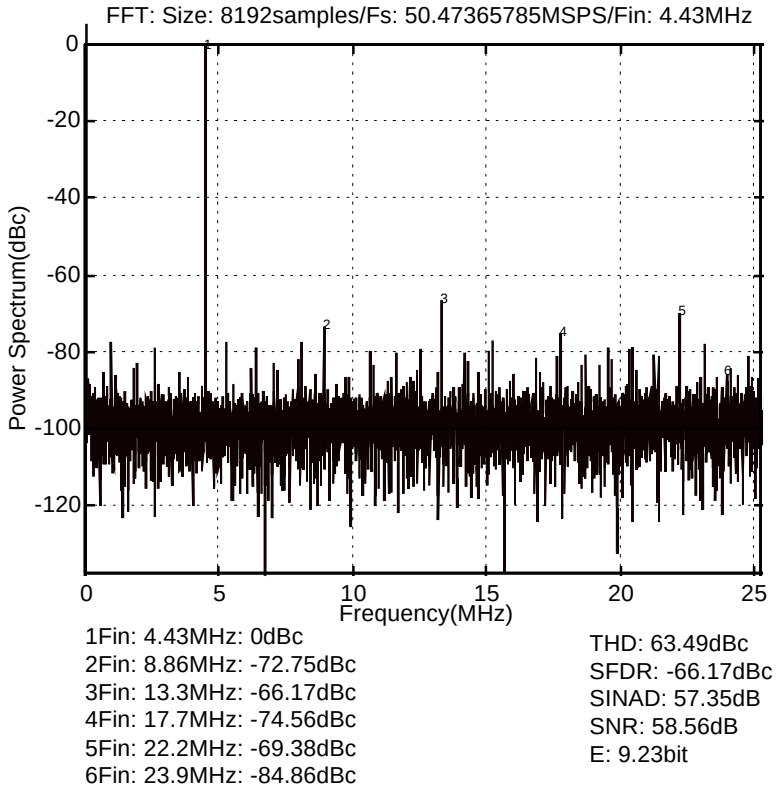
- Figure 22. Results of the 40Msps version -

8.4 MEASUREMENT OF THE 50MSPS VERSION:

This version of the **Demoboard** is evaluated with the following measurement conditions:

Input frequency:	4.43MHz.
Waveform:	Sinus.
Magnitude:	Full Scale.
Antialiasing Filter:	Yes.
Clock frequency:	50.474Msps.
Operating mode:	External clock.

The typical results and the corresponding diagram obtained with these conditions are given on **Figure 23**:



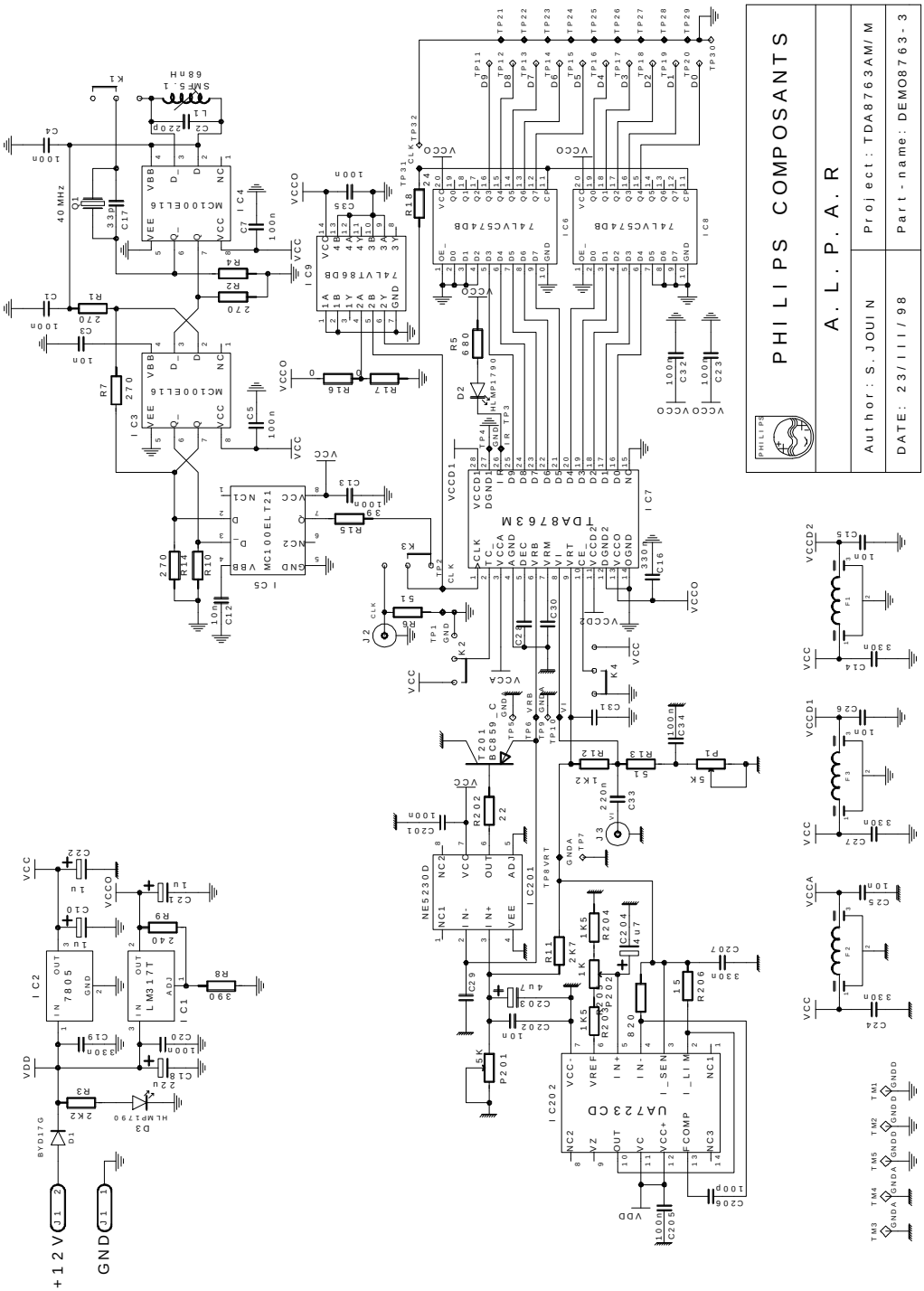
- Figure 23. Results of the 50Msps version -

9. DEMOBOARD FILES:

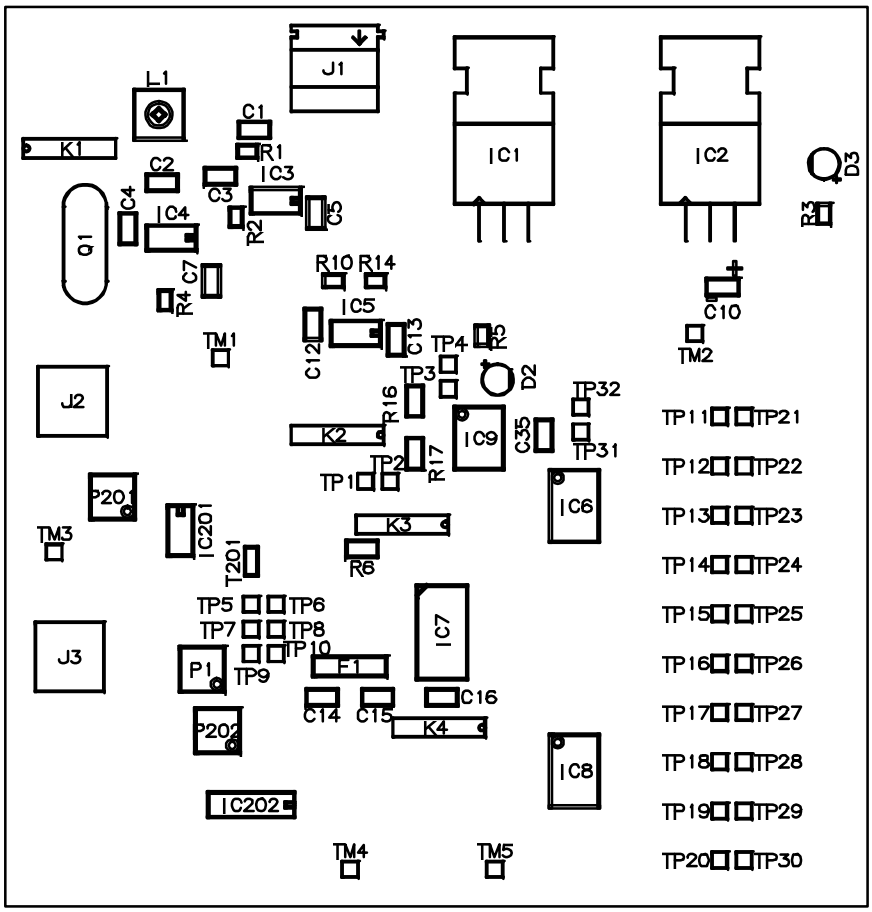
All documents needed for the realization of this **Demoboard** are given from **Figures 24 to 31**.

- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside component layout 1.
- Internal layout ground layout 2.
- Internal layout supply layout 3.
- Internal layout ground layout 4.
- Underside component layout 5

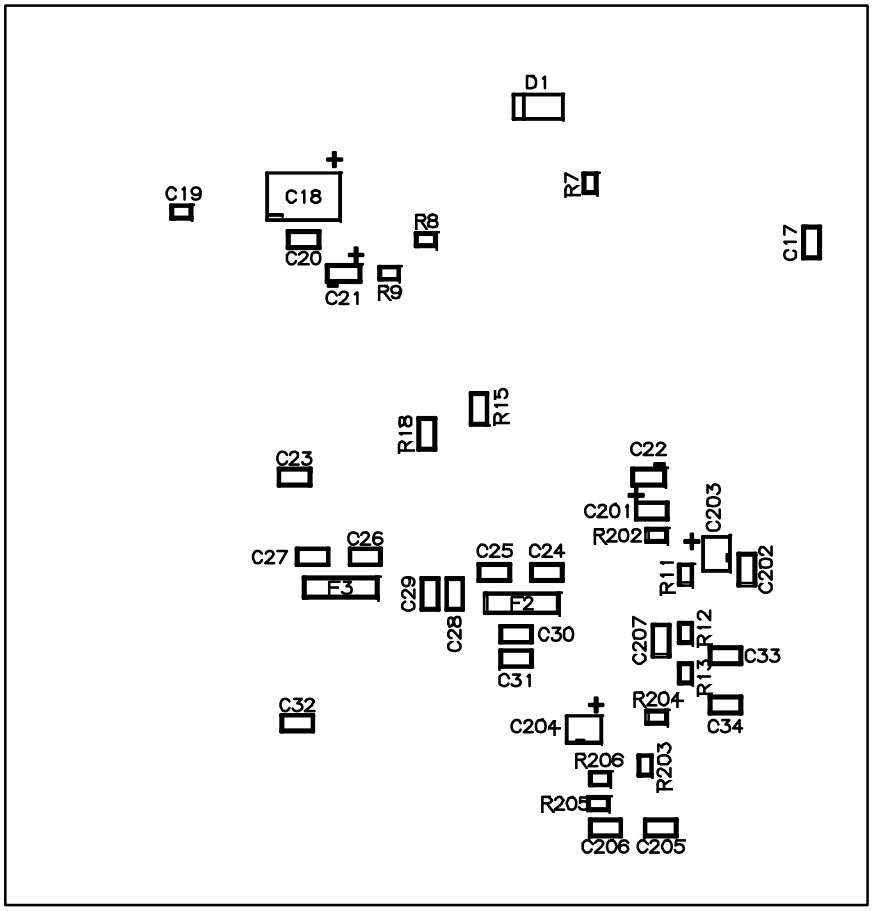
The list of components with their values and references is given from **Table 1 to 3**. The list of extra components with their values and references for the **TDA8763AM** version is given on **Table 4**.



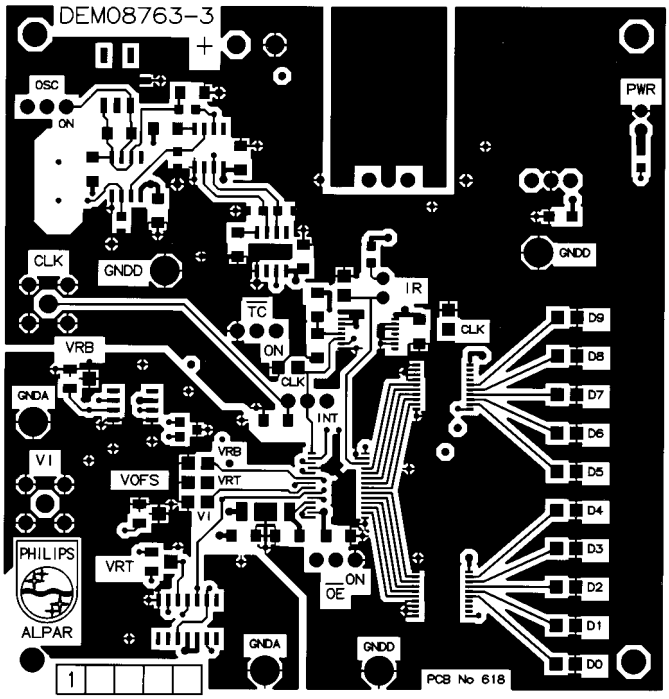
- Figure 24. Demoboard electrical diagram -



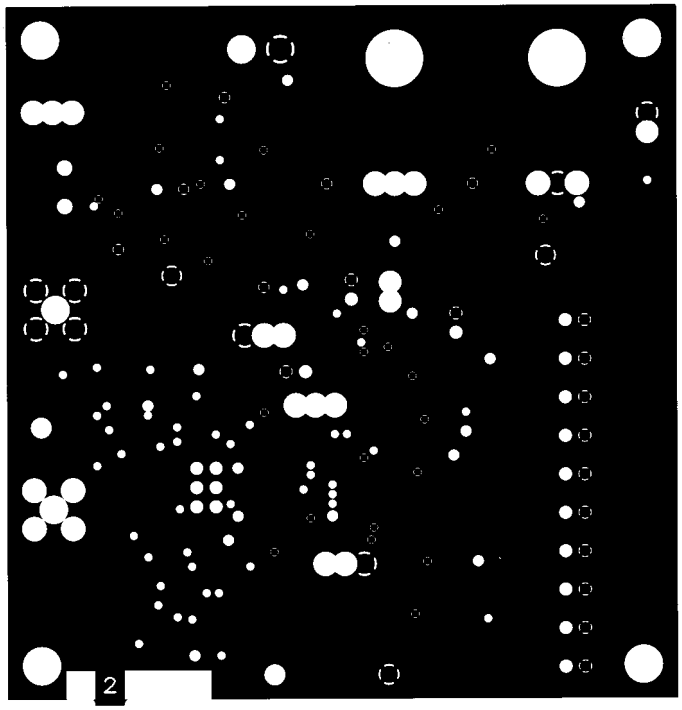
- Figure 25. Topside component implantation -



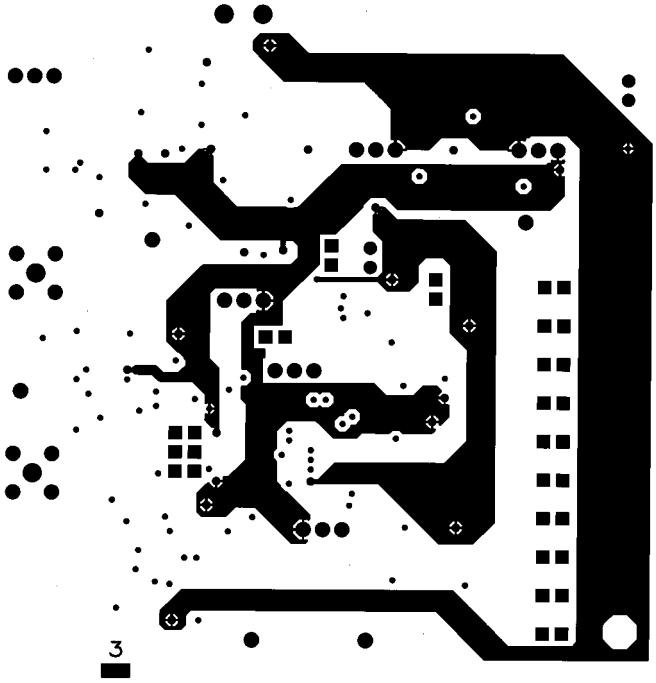
- Figure 26. Underside component implantation -



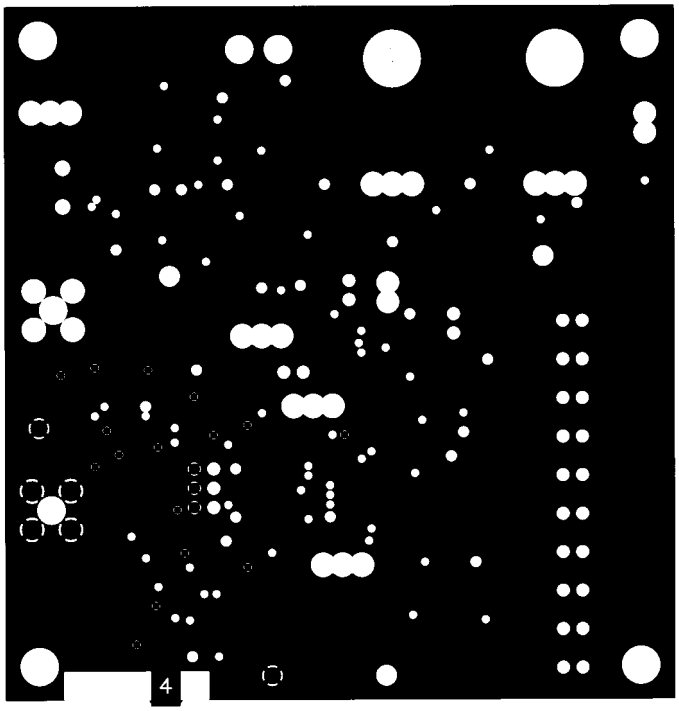
- Figure 27. Topside component layout (signal layer 1) -



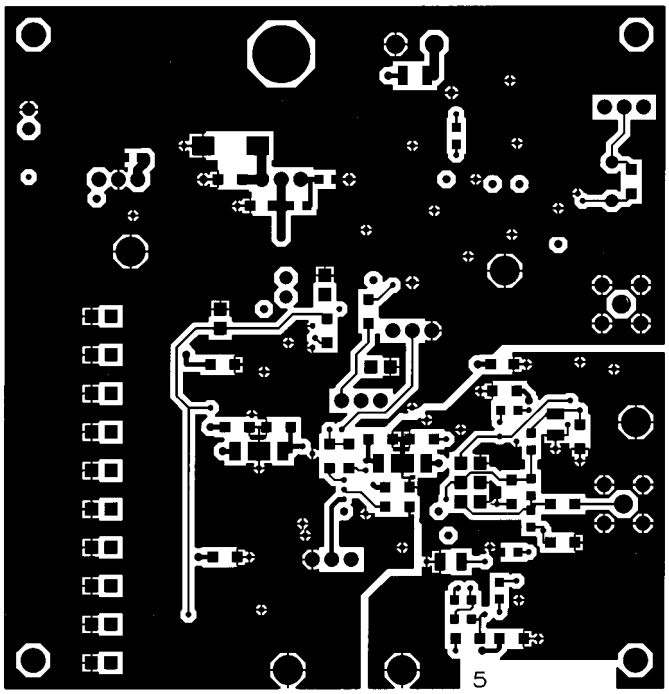
- Figure 28. Internal plane layout (ground layer 2) -



- Figure 29. Internal layout (supply layer 3) -



- Figure 30. Internal plane layout (ground layer 4) -



- Figure 31. Underside component layout (signal layer 5) -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C1	100nF	CAPACITOR	C1206	PHILIPS
C2	390pF/220pF/120pF	'	'	'
C3	10nF	'	'	'
C4	100nF	'	'	'
C5	100nF	'	'	'
C7	100nF	'	'	'
C10	1µF/16V	'	293D/A	SPRAGUE
C12	10nF	'	C1206	PHILIPS
C13	100nF	'	'	'
C14	330nF	'	'	'
C15	10nF	'	'	'
C16	330nF	'	'	'
C17	33pF	'	'	'
C18	22µF/16V	'	293D/D	SPRAGUE
C19	330nF	'	C0805	PHILIPS
C20	100nF	'	C1206	'
C21	1µF/16V	'	293D/A	SPRAGUE
C22	1µF/16V	'	'	'
C23	100nF	'	C1206	PHILIPS
C24	330nF	'	'	'
C25	10nF	'	'	'
C26	10nF	'	'	'
C27	330nF	'	'	'
C28(1)	NC/4,7nF	'	'	'
C29(1)	100nF/1nF	'	'	'
C30(1)	100nF/1nF	'	'	'
C31	100nF	'	'	'
C32	100nF	'	'	'
C33	220nF	'	'	'
C34	100nF	'	'	'
C35	100nF	'	'	'
D1		DIODE	BYD17G	PHILIPS
D2		RED LED	HLMP1790	HEWLETT PACKARD
D3		GREEN LED	HLMP1790	'
F1	2nF	Π FILTER	4700-003-S	TUSONIX
F2	2nF	'	'	'
F3	2nF	'	'	'

(1): TDA8763AM/TDA8763M version.

- Table 1. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
IC1		ADJUSTABLE REGULATOR	LM317T	TEXAS INSTRUMENTS
IC2		VOLTAGE REGULATOR	T7805CT	MOTOROLA
IC3		LINE RECEIVER	MC100EL16	"
IC4		"	MC100EL16	"
IC5		PECL TO ECL TRANSLATOR	MC100ELT21	"
IC6		D TYPE FLIP FLOP	74LVT574DB	PHILIPS
IC7		ADC	TDA8763AM/TDA8763M	"
IC8		D TYPE FLIP FLOP	74LVT574DB	"
IC9		EXCLUSIVE-OR	74LVT86DB	"
J1		CONNECTOR	MKSD	PHOENIX
J2	50Ω	"	SMA	RADIALL
J3	50Ω	"	‘	‘
K1		SWITCH	1C2P	SECME
K2		"	"	"
K3		"	"	"
K4		"	"	"
L1	68nH	SELF	SMF5.1	NEOSID
P1	5KΩ	POTENTIOMETER	3224W	BOURNS
Q1	32MHz/40MHz/50MHz	QUARTZ	HC49U	KONY
R1	270Ω	RESISTOR	0805	PHILIPS
R2	270Ω	"	"	"
R3	2.2kΩ	"	"	"
R4	270Ω	"	"	"
R5	680Ω	"	"	"
R6	51Ω	"	1206	"
R7	270Ω	"	0805	"
R8	390Ω	"	"	"
R9	240Ω	"	"	"
R10	270Ω	"	"	"
R12	1.2kΩ	"	"	"
R13	51Ω	"	"	"
R14	270Ω	‘	‘	‘
R15	39Ω	"	1206	"
R16(1)	0Ω/NC	‘	‘	‘
R17(1)	NC/0Ω	‘	‘	‘

(1): TDA8763AM/TDA8763M version.

- Table 2. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
R18	24Ω	RESISTOR	1206	PHILIPS
R24	62Ω	"	"	"
TM1		MEASUREMENT POINT		COMATEL
TM2		"		"
TM3		"		"
TM4		"		"
TM5		"		"
TP1		TEST POINT		COMATEL
TP2		"		"
TP3		"		"
TP4		"		"
TP5		"		"
TP6		"		"
TP7		"		"
TP8		"		"
TP9		"		"
TP10		"		"
TP11		"		"
TP12		"		"
TP13		"		"
TP14		"		"
TP15		"		"
TP16		"		"
TP17		"		"
TP18		"		"
TP19		"		"
TP20		"		"
TP21		"		"
TP22		"		"
TP23		"		"
TP24		"		"
TP25		"		"
TP26		"		"
TP27		"		"
TP28		"		"
TP29		"		"
TP30		"		"
TP31		"		"
TP32		"		"

- Table 3. List of components -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C201	100nF	CAPACITOR	C1206	PHILIPS
C202	10nF	'	'	'
C203	4.7µF/16V	'	293D/B	SPRAGUE
C204	4.7µF/16V	'	'	'
C205	100nF	'	C1206	PHILIPS
C206	100pF	'	'	'
C207	330nF	'	'	'
IC201		LOW VOLTAGE OP. AMPLI.	NE5230D	PHILIPS
IC202		PRECISION VOLTAGE REG.	UA723CD	'
P201	5KΩ	POTENTIOMETER	3224W	BOURNS
P202	1KΩ	'	'	'
R11	2.7KΩ	RESISTOR	0805	PHILIPS
R202	22Ω	'	'	'
R203	1.5KΩ	'	'	'
R204	1.5KΩ	'	'	'
R205	820Ω	'	'	'
R206	15Ω	'	'	'
T201		TRANSISTOR PNP	BC859C	PHILIPS

- Table 4. List of components for the TDA8763AM version only -